What is claimed is:

1. A semiconductor device comprising:

a carrier substrate;

a temperature sensing resistive element deposited on the carrier substrate;

a semiconductor element mounting portion laid on the carrier substrate; and

a semiconductor element mounted on the semiconductor element mounting portion.

2. A semiconductor device according to claim 1, wherein the carrier substrate is formed of ceramics.

3. A semiconductor device according to claim 1, further comprising conductive patterns that are formed on the carrier substrate and connected with the temperature sensing resistive element.

4. A semiconductor device according to claim 3, wherein each of the conductive patterns has a bonding point that is electrically connected to an outside, and has a portion having low thermal conductivity between the bonding point and the temperature sensing resistive element.

5. A semiconductor device according to claim 4, wherein the portion having the low thermal conductivity is a bent portion of each of the conductive patterns.

6. A semiconductor device according to claim 4, wherein the portion having the low thermal conductivity is a small width portion of each of the conductive

patterns.

7. A semiconductor device according to claim 1, wherein the temperature sensing resistive element contains at least one of Mn, Ni, Co, and Fe.

8. A semiconductor device according to claim 1, wherein the semiconductor element is a semiconductor laser.

9. A semiconductor device according to claim 8, wherein a heat sink is interposed between the semiconductor laser and the mounting portion.

10. A chip carrier comprising:

a carrier substrate;

a temperature sensing resistive element deposited on the carrier substrate; and

a semiconductor element mounting portion laid on the carrier substrate.

11. A chip carrier according to claim 10, wherein the carrier substrate is formed of ceramics.

12. A chip carrier according to claim 10, further comprising conductive patterns that are formed on the carrier substrate and connected to the temperature sensing resistive element.

13. A chip carrier according to claim 12, wherein each of the conductive patterns has a bonding point that is electrically connected to an outside, and has a portion having low thermal conductivity between the bonding point and the temperature sensing resistive

element.

14. A chip carrier according to claim 13, wherein the portion having the low thermal conductivity is a bent portion of each of the conductive patterns.

15. A chip carrier according to claim 13, wherein the portion having the low thermal conductivity is a small width portion of each of the conductive patterns.

16. A chip carrier according to claim 10, wherein the temperature sensing resistive element is formed through a step of sintering on the carrier substrate.

17. A chip carrier according to claim 16, wherein the temperature sensing resistive element contains at least one of Mn, Ni, Co, and Fe.